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An Approach for Synchronization in Carrier Signal with Noise Distortion Using Complex Binary Phase Locked Loop Method

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Abstract: *In this paper Phase estimation and carrier synchronization have been envisaged using complex binary phase locked loop. The same is also studied for a noise corrupted signal. This was found out that complex binary number is well suited for demodulation. The approach has been for complex signal which has carrier signal and information signal whose synchronization is required with noise in the receiver end.*

Keywords: *Complex digit, phase locked loop, additive noise, synchronization, quadrature, investigation.*

1. INTRODUCTION

There are two basic approaches for carrier synchronization at the receiver. In one approach a pilot signal is carrier frequency and phase of received signal. In the second approach a phase locked loop is employed at the receiver for carrier synchronization. This method has the advantage that the total transmitted power is allocated to the transmission of the information bearing signal. Carrier recovery and timing synchronization have been thoroughly investigated our past three decades. The analog and digital implementations of PLL's have been studied by Gupat [1] and Lindsey and Chie[2]. Comprehensive treatments of phase locked loops have been appeared in the book of Proakis[3] and references there in. The investigation of complex binary digit was first performed by Pekmestzi[4].

In this paper our main aim is to study phase locked loops for a complex binary digit. This is a straight forward approach to extract the carrier. The advantage of this approach is that the complex binary signal always requires a complex valued quantity i.e. the complex carriers and complex filters. The hardware realization is the same as two real binary numbers in phase quadrature but complex number multiplication through complex binary takes half the time than that of conventional binary. It reduces the circuit complexity for implementation of multiplication and arithmetic operation.

2. PHASE LOCKED LOOP

Block diagram of phase locked loop for carrier recovery is shown in Fig. l. The amplitude modulated signal with the phase ϕ is multiplied by the complex carrier signal with phase $\hat{\phi}$. The result is a complex signal and this signal is allowed to pass through a low-pass filter. The output of filter is a complex signal having a phase difference $\phi - \hat{\phi}$. After that the complex phase signal is allowed to pass through loop filter and the output of filter produces the signal which is the input for voltage controlled oscillator. The output of VCO produces a complex carrier. The circuit is similar to conventional binary amplitude modulation. Thus, we find that carrier recovery is achieved in the simple way while the hardware realized to generate complex signal is same as two signals wish phase quadrature. The process can be explained mathematically which is as follows:

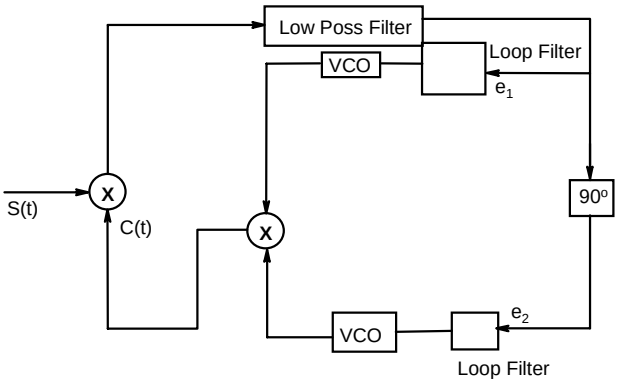

Figure 1: Block Diagram of Phase Locked Loop for Complex Binary Digit

Let the amplitude modulated complex binary digit can be represented by

$$S(t) = (A_r + jB_i)\, e^{j(\omega ct+\phi)} \quad (1)$$

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where A_r and B_i are real and imaginary amplitudes respectively, ϕ is phase angle.

We now Consider a Carrier of Complex Valued quantity which is as follows.

$$C(t) = e^{-j}(\omega_c t + \hat{\phi}) \quad (2)$$

Multiplying equation (1) and (2) and solving, we have

$$C(t)\cdot S(t) = (A_r + j\,B_i)\cos(2\omega_c t + \phi + \hat{\phi} + \text{Cos}$$

$$(\phi - \hat{\phi}) - j\,(A_r + j\,B_i)\,\text{Sin}\,(2\omega_c t + \phi + \hat{\phi}) -$$

$$\text{Sin}\,(\phi - \hat{\phi}) + (j\,A_r + B_i)\,\text{Sin}\,(2\omega_c t + \phi + \hat{\phi}) - \text{Sin}\,(\phi - \hat{\phi})$$

$$-(A_r + j\,B_i)\cos(2\omega_s t + \phi + \hat{\phi}) + \text{Cos}\,(\phi - \hat{\phi}) \quad (3)$$

After low Pass filtering the above signal is reduced to

$$e(t) = 2\,(A_r + jB_i)\,[\text{Cos}(\phi - \hat{\phi}) + j\,\text{Sin}\,(\phi - \hat{\phi})] \quad (4)$$

or $$e\,(t) = e_1(t) + e_2(t) \quad (5)$$

where $$e_1 = 2(A_r + j\,B_i)\,\text{Cos}\,(\phi - \hat{\phi}\,) \quad (6)$$

and

$$e_2 = 2(A_r + jB_i)\,\text{Sin}\,(\phi - \hat{\phi}) \quad (7)$$

These are required Signals which are allowed to through VCO'S.

3. ANALYSIS OF PLL

The Mathematical analysis of Phase Locked loop can be performed as.

Phase angle difference is given

$$\phi = \hat{\phi} = \psi$$

Or

$$\psi = \phi - G_o \int_{-\infty}^{t} V_o(\lambda)d\lambda \quad (1)$$

where $$\phi = \text{G}_\text{o} \int_{-\infty}^{t} V_o(\lambda)d\lambda$$

and G_o is a Constant Which Shows Change in insaneness frequency.

V_o is output Voltage of L.P. filter.

Differentiating w.r. to, t, we have

$$\frac{d\Psi}{dt} + GV_0 = \frac{d\phi}{dt} \quad (2)$$

Here,

$$V_0 = 2(A_r + jB_i)\cos(\phi - \hat{\phi}) + j\,\sin(\phi - \hat{\phi}) \quad (3)$$

Replacing the sinusoidal and co-sinusoidal variation from equation (3) by piece wise linear variation, we get

$$V_0 = 4(A_r + jB_i)\,G_P\left(1 - \frac{\Psi}{\pi/2}\right) + j\left(\frac{\Psi}{\pi/2}\right) \text{ for } \psi \le \pi/2 \quad (4)$$

where G_P is gain of the filter.

New equation (4) can be written as

$$V_0 = V_{01} + V_{02} \quad (5)$$

where $$V_{01} = 4A_r\,G_P\left(1 - \frac{\Psi}{\pi/2}\right) \quad (6)$$

and $$V_{02} = 4B_1\,G_P\frac{\Psi}{\pi/2} \quad (7)$$

For $V_{02'}$ 1st order filter equation is given by,

$$\frac{d\Psi}{dt} + \frac{\Psi}{\tau} = \frac{d\phi}{dt} \quad (\psi \le \pi/2) \quad (8)$$

where $\tau = \dfrac{\pi}{8G_0G_PB_i}$

For V_{01}, 1st order filter equation is given as –

$$\frac{d\Psi}{dt} + \frac{x}{2\tau'} - \frac{\Psi}{\tau'} = \frac{d\phi}{dt} \quad (9)$$

where $\tau = \dfrac{\pi}{8G_0G_PB_r}$

From equation (8) and (7), we have

$$\frac{dV_{02}}{dt} + \frac{V_{02}}{\tau} = \frac{1}{G_0\tau}\frac{d\phi}{dt} \quad (10)$$

From equation (6) and (9), we have

$$\frac{dV_{01}}{dt} + \frac{\pi}{2G_0\tau'^2} = \frac{V_{01}}{\tau'} = \frac{1}{G_0\tau'}\frac{d\phi}{dt} \quad (11)$$

Equation (10) and (11) are the differential equations of PLL. Following the method[3] we can easily obtain the transfer functions which are as follows

$$H_1(s) = \frac{1}{s + \frac{1}{\tau}} \quad (12)$$

which is the same as for ordinary PLL.

and $$H_2(s) = \frac{1-k}{s - \frac{1}{\tau'}}$$

where $$K = \frac{\pi}{2\tau\Omega(s)} \quad (13)$$

4. PLL MODEL 1 WITH ADDITIVE NOISE

The phase locked loop mode 1 with additive noise system is shown in fig. (2). The noise corrupted complex signal having an instantaneous phase ϕ is multiplied by the complex carrier with phase $\hat{\phi}$ produced by a VCO and the frequency term is neglected, here the input to the loop filter is noise corrupted signal. The process can be mathematical explained as.

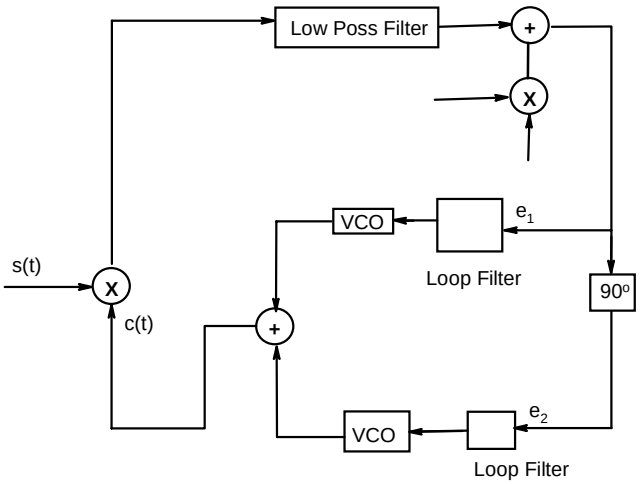

Figure 2: Block Diagram of PLL with Noise

The signal is represented by

$$s(t)+n(t)=(A_r+jB_i)\,e^{-j(\omega_c t+\phi)}+n_c(t)\,\text{Cos}\,(\omega_c t+\phi) - n\,\text{Sin}\,(\omega_c t+\phi) \quad (1)$$

where $n(t)$ is noise

The carrier is given by

$$c(t)=e^{-j(\omega_c t+\hat{\phi})} \quad (2)$$

Multiplying (1) and (2) and then filtering, we have

$$e(t)=2(A_r+jB_i)\,\text{Cos}\,(\phi-\hat{\phi})+j\,\text{Sin}\,(\phi-\hat{\phi}) + (n_S+j\,n_S)\,\text{Cos}\,(\phi-\hat{\phi})+j\,\text{Sin}\,(\phi-\hat{\phi}) \quad (3)$$
$$=e_1(t)+e_2(t)$$

where

$$e_1=2(A_r+jB_i)+\frac{1}{2}(n_C+jn_S)\times\text{Cos}\,(\phi-\hat{\phi}) \quad (4)$$

$$e_2=2(A_r+jB_i)+\frac{1}{2}(n_c+j\,n_S)\,\text{Sin}\,(\phi-\hat{\phi}) \quad (5)$$

These are the required noise corrupted inputs applied to VCO'S.

5. Conclusion

Complex binary can be directly implemented for phase locked loop like simple binary for a complex signal. It requires a little modification in the convention circuit of PLL. It requires two VCO's and two loop, –filters and one additional adder and remaining circuits are similar to simple PLL. Due to modular type multipliers and adders[4], the complexity of circuit is minimized and faster communication is possible. We find that complex binary is very suitable for faster communication and VLSI circuit realization. Complex binary can be directly employed in quadrature phase shift keying.

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A phase locked loop (PLL) operates on the serialized received modulation symbols and provides an independent phase correction value for each received modulation symbol. Each received modulation symbol is corrected with its own phase correction value to obtain a phase-corrected symbol. The phase error in each phase-corrected symbol is detected to obtain a phase error estimate for that phase-corrected symbol.Â An Approach for Synchronization in Carrier Signal with Noise Distortion Using Complex Binary Phase Locked Loop Method. Krishna Chandra Roy, Manoj Kumar, Ashok Kumar. IJEE. Traditionally, carrier synchronization is achieved by a carrier tracking loop, which is often implemented as PLL.Â A method to determine appropriate loop noise bandwidth is considering the worst carrier-to-noise power density ratio (CNR) and max relative dynamic (i.e., max relative acceleration for the 2nd-order PLL and max relative jerk for the 3rd-order PLL) [4]. Unfortunately, it will lead to a suboptimal loop for low relative dynamic.Â When PLL is in a locking state, the received carrier phase can be measured by observing the local generated carrier. Meantime, the carrier is wiped off from the received signal. Figure 1 shows the traditional linear PLL model.Â The phase difference is sent into the loop filter which not only filters the noise but also generates the control signals to NCO.